WAVECREST Corporation

Characterizing AC Timing and Jitter Generation on Low Voltage Differential Swing (LVDS) Transmitters

Application Note No. 131

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Introduction

The need for larger bandwidth in data communications, microprocessor systems, multi-media and networking applications continues with no foreseable upper limit. Low Voltage Differential Swing components try to address the need for high speeds (>200MB/s) and low power consumption while accommodating a wide range of applications. There are two industry standards that define and govern LVDS technology. The first is the ANSI/TIS/EIA-644 standard developed under the Data Transmission committee TR3.02. This is the standard that defines the driver and receiver I/O characteristics. The purpose of this committee is to establish standards that work up to the theoretical limit of 1.923GB/s. The second standard that parts using LVDS buffers must adhere to is the IEEE 1596.3 SCI-LVDS which specifies the signal levels for the physical layer interface and defines encoding for packet switching.

This paper will document the use of *WAVECREST*'s DTS-2077™ to measure LVDS specification standards for signal levels, rise time, propagation delay, jitter transfer and jitter generation. This paper is general purpose in tone and other applications should find these techniques valuable.

Engineers who want to learn more about taking measurements of any type of differential signal as well as those who want to take rise time measurements, calibrate test fixtures for propagation delays and take general, two-channel measurements on DTS instruments will find this application note useful. Engineers needing an introduction to jitter generation, dataCOM and Tail-fit™ measurement techniques or those interested in correlation to bench instrumentation will also find useful information in this paper.

Background

Differential signals have tremendous advantages over single-ended schemes. Differential signals are practically immune to the common-mode noise seen in point-to-point communications. Crosstalk noise coupled onto interconnects is seen by a differential receiver as a common mode modulation between the + and – inputs and is rejected. Differential receivers only respond to the differential voltages. This common mode noise rejection eases the noise burden of the transmission media providing significant cost savings in system designs. LVDS, with its low signal level (+/-400 mv) around differential 0 volts, can achieve data rates up to 1000MB/s using CMOS technology.

Testing LVDS Drivers

LVDS components use constant current mode drivers that provide a maximum 4.5mA source current. Using a current mode driver forces proper termination of the transmission media. Ideally, the transmission media should be terminated to the characteristic impedance of the driver. Typically, this is 100-120Ω and is matched to the cable. A termination resistor is *required* to generate the differential output voltage (Vod) at the receiver input. Figure 1 shows the proper termination scheme for an LVDS buffer.

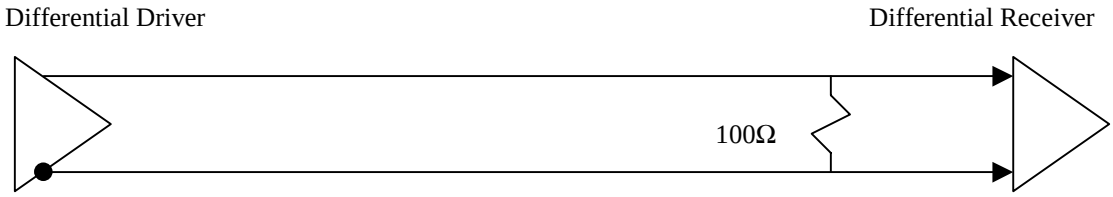


Figure 1 - LVDS Termination Scheme

This termination scheme presents some problems for instruments that terminate the inputs with 50Ω to ground. If connected directly, the impedance load seen by the part is shown in Figure 2.

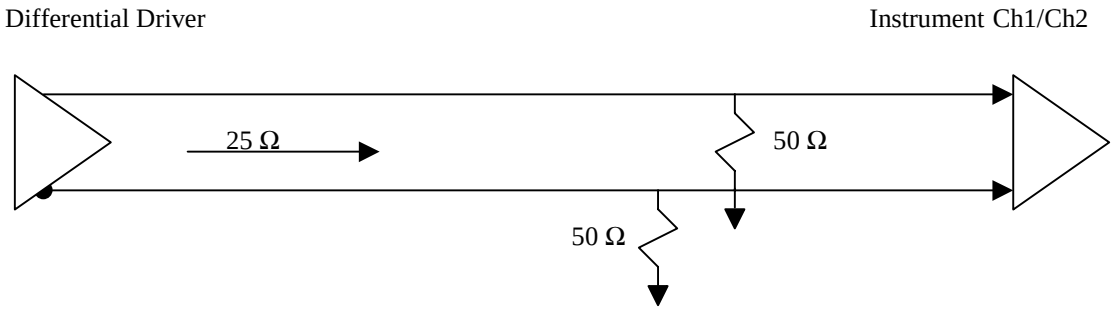


Figure 2 - Termination Scheme Achieved with 50Ω Terminations at Receiver Inputs

The LVDS device sees an equivalent 25Ω to GND termination on the differential outputs. The LVDS performance will be drastically compromised when terminated in this manner as well as most ATE comparators, 50Ω high speed sampling heads used by DSOs and the *WAVECREST* DTS-2077™.

The output signals of the LVDS part under this load are shown in Figure 3.

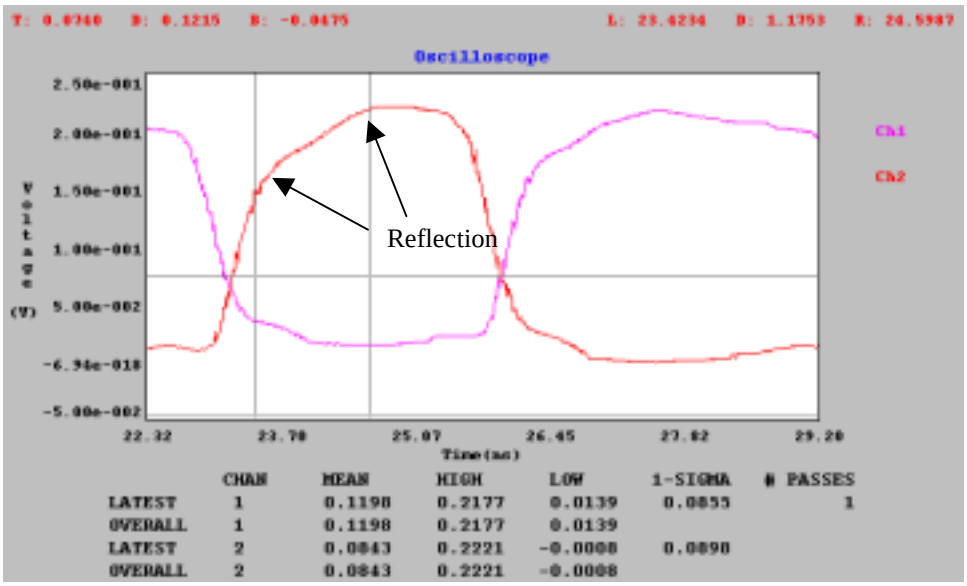


Figure 3 - LVDS outputs into 50Ω Load

Note the presence of a large reflection on the signal lasting 1.17ns. Without proper termination, components lose the effectiveness of the termination resistor to act as a pull-up and sink the 4.5mA drive current.

Termination to 100 Ohms

In Figure 4, the LVDS driver is terminated to 100Ω and each of the differential outputs is input to the DTS-2077™.

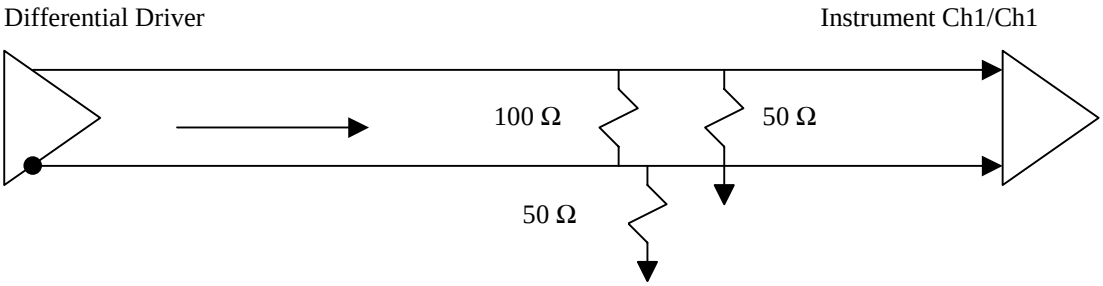


Figure 4 - 100Ω Termination into 50Ω

The impedance seen by the differential outputs looks like 100Ω in parallel with 50Ω, which is equal to 33Ω, then 33Ω in parallel with 33Ω, or 18.5Ω. This results in impedance too low to properly match the outputs driving a 50Ω transmission line and produces the large signal overshoot shown in Figure 5.

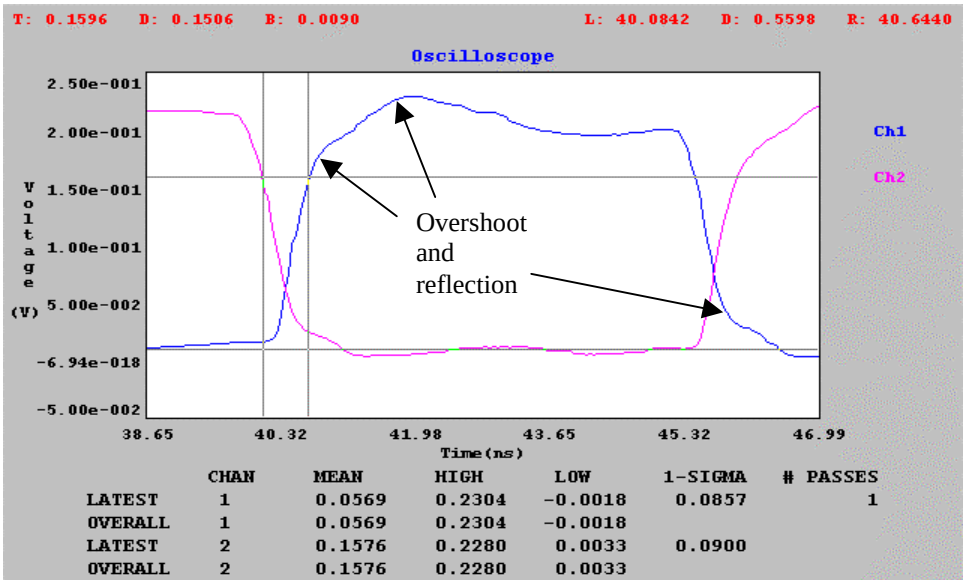


Figure 5 - Differential outputs with 100Ω termination seen into 50Ω

This type of termination might perform better than the 50Ω-to-GND setup if forced by setup conditions, but a signal with this type of overshoot can understate rise time and produce a large differential zero crossing skew. Also, propagation delay measurements will be in error. Using this termination in a production setting is not recommended.

The proper termination setup for accurately measuring LVDS differential outputs is shown in Figure 6.

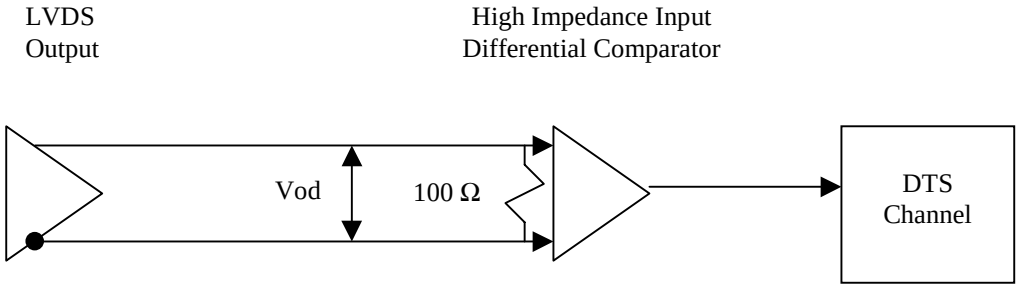


Figure 6 - Proper Measurement Setup for LVDS

Essentially, the differential comparator is a unity gain op-amp providing a high impedance load for the measurement circuitry while the 100Ω resistor provides the proper load for the current mode drivers. When this termination scheme is followed, the signal is very clean and proper measurements can be made. Figure 7 shows the resulting differential swing using Tektronix P6247 Differential Probes acting as the comparator. These probes provide over 1GHz bandwidth, less than 1pf of differential load capacitance and good frequency response through the LVDS frequency bands[2]. The LVDS device being used is specified to 400MB/s, so the P6247 probe is ideal for this application.

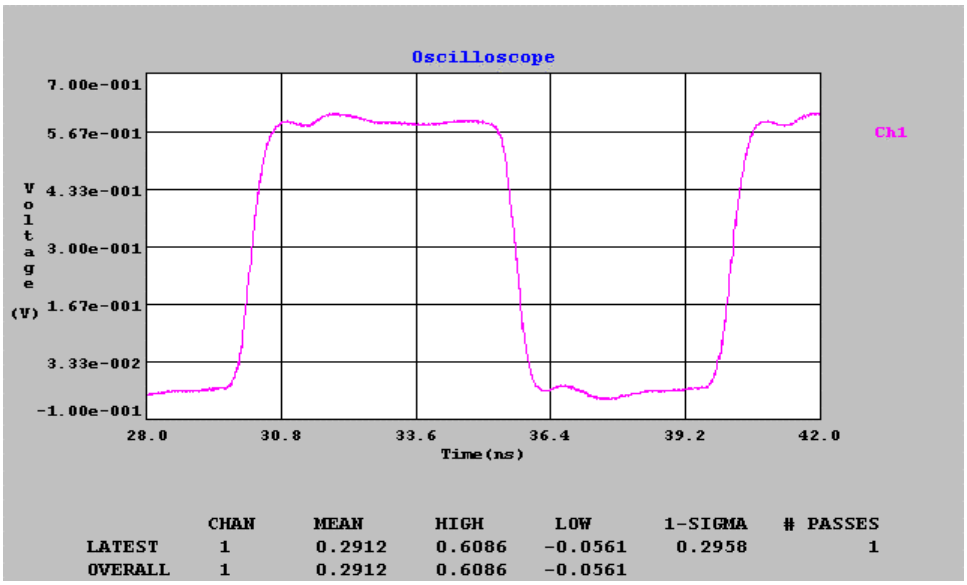


Figure 7 - Differential Output using P6247 Probe and 100Ω Termination and Measured Single Ended

Using a differential receiver to produce high impedance measurement loading as well as isolating the 50Ω input impedance is the recommended method for interfacing LVDS transmitters to the DTS-207x instrument in production and high accuracy characterization applications.

Measuring Differential Rise/Fall Time

A critical specification for LVDS drivers is the differential Rise/Fall time and is defined as the time it takes to transition the 20% to 80% differential voltages measured from differential 0V (See Figure 8), the rise time that a differential receiver acts upon.

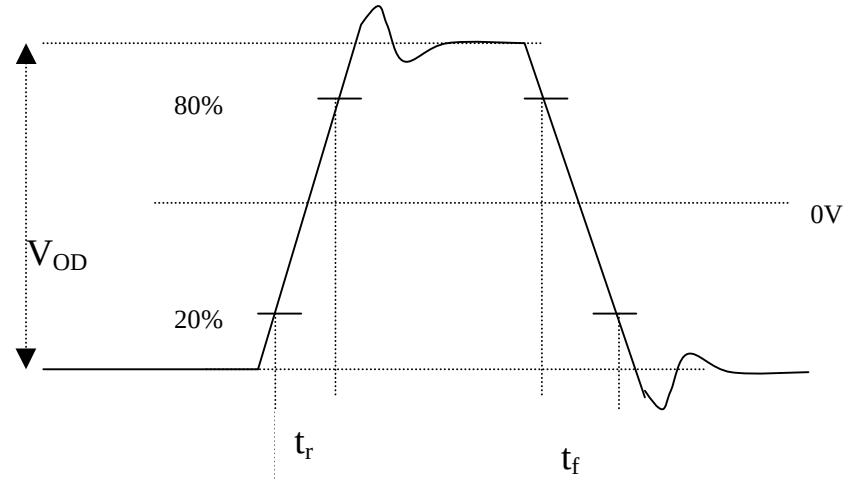


Figure 8 - T_{rise} and T_{fall}

Rise and Fall times are critical timing parameters since this specification determines the buffer circuit's ability to operate at high frequencies, enables the buffer to drive less than optimum media and provides the margin that enables devices to operate beyond rated specifications. Figure 9 is a Virtual Instrument™ Oscilloscope display of Vod at the 20%-80% time.

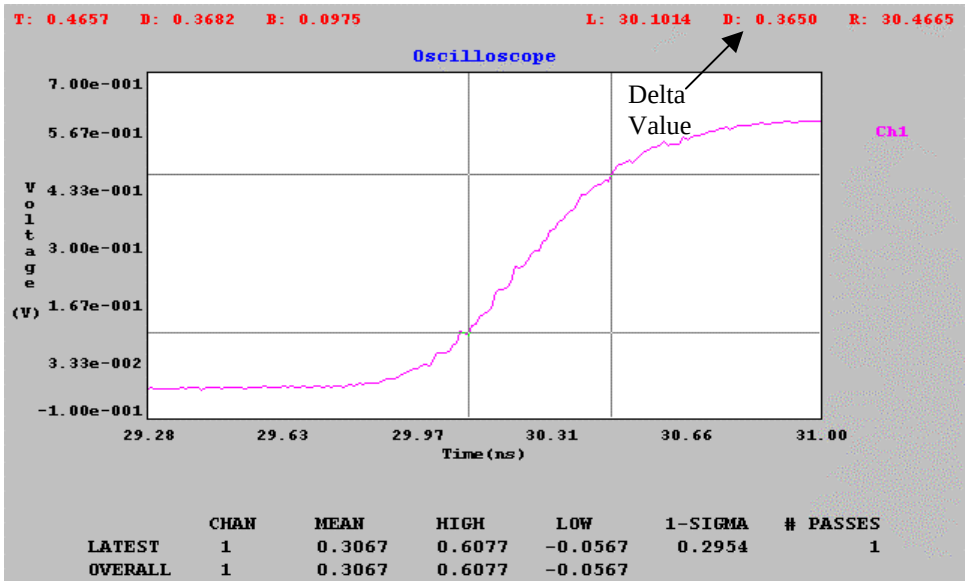


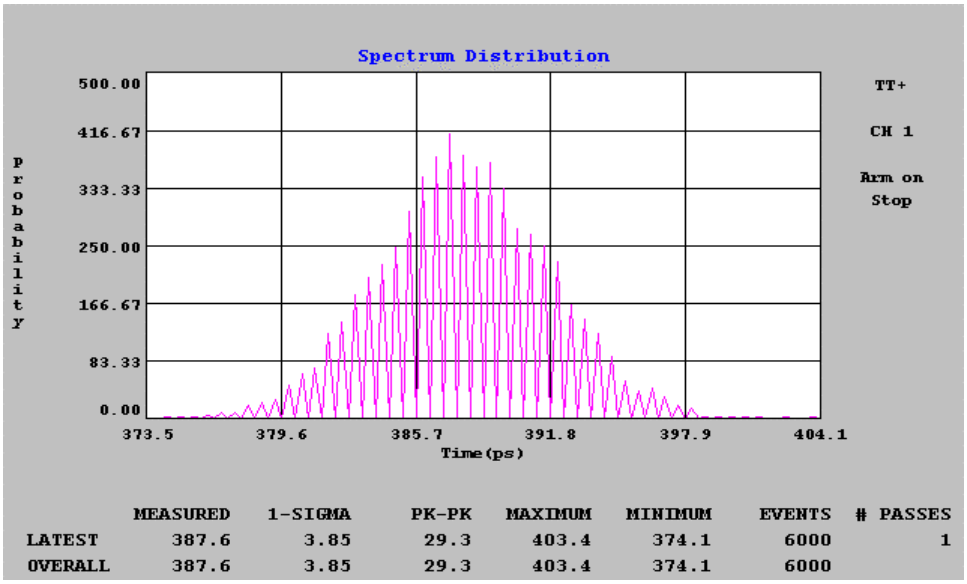
Figure 9 - Rise Time in Oscilloscope Tool

The rise time measured by the markers at the 20%-80% point is 365ps. This value is shown in red in the upper right hand corner of the plot as the D (delta) value. This measurement is accurate to 10ps. The Oscilloscope tool would not normally be used to measure rise time.

Histogram Tool Measurement

A faster and much more accurate way to take measurements on the DTS-2077™ is by using the Spectrum tool. The Spectrum tool produces highly accurate histograms very quickly. Figure 10 is a simple histogram plot using the following setup in the Function Dialog pull-down menu of the Spectrum Tool:

Function..... TT+ (*Transition Time Positive or Rise Time)*
Channel..... 1
Start Voltage..... 0.0975
Stop Voltage..... 0.4657
Sample Size..... 6000
Pulse Find %..... USER
Arming..... Arm on Start
Start Arming Event 1
Stop Arming Event 1



	MEASURED	1-SIGMA	PK-PK	MAXIMUM	MINIMUM	EVENTS	# PASSES
LATEST	387.6	3.85	29.3	403.4	374.1	6000	1
OVERALL	387.6	3.85	29.3	403.4	374.1	6000	

Figure 10 - Rise Time Histogram

This plot has very good correlates the measured values with the scope plot in Figure 9. Remember that the measurement of rise time taken with an oscilloscope will be a look at one edge in time that biases the measurement to the trigger signal and minimizes the rise time errors. Plotting the rise times at random intervals exposes all the linearity errors while keeping the measurement free from trigger bias.

The histogram measures 387ps and represents the mean of the 6000 measurements taken. The 1-sigma (3.85ps) is calculated from 6000 measurements. The peak-to-peak (29.3ps) value is the difference between the Maximum and Minimum values found in the measurement population of 6000.

Setting the Comparator Voltages Properly

Correlating rise times between test equipment can be difficult. Differences in analog bandwidth, voltage reference accuracy and the comparator trip algorithm used to set the levels at 20%-80% of the full voltage swing all contribute to inaccuracies. In order to use the DTS-2077™ properly and be able to correlate the measurements to a high-bandwidth DSO, properly setting the comparator levels on the DTS-2077 is important.

The scope display in Figure 11 is a plot using a CS803A (11801) Tektronix Oscilloscope with a 20GHz plug-in. The same differential probes were used to measure rise time on this scope. The voltages measured with a 20GHz bandwidth are now correct for rise/fall times.

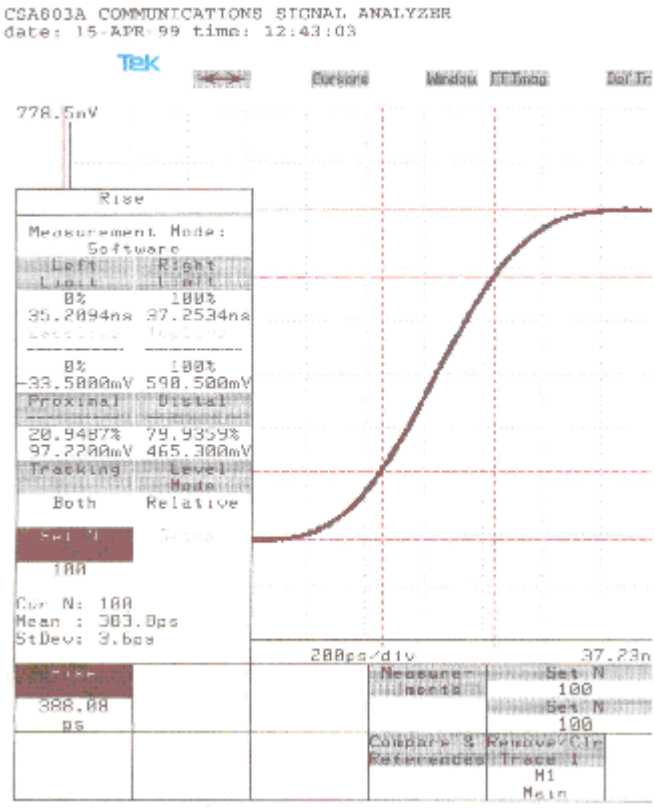


Figure 11 -CS803A Rise Time Measurement

Rise Time Results

The rise time measured by the CS803A, which has a 20GHz analog bandwidth, is very close to the rise time seen by the DTS-2077™ and *Virtual Instruments*™ Histogram tool.

CS803A	DTS-2077 Histogram	DTS-2077 Oscilloscope
388.00ps	387.6ps	365ps

Table 1 - Rise Time Correlation

The difference in results from the DTS-2077 scope and both the CS803 and DTS-2077 histogram is due to the DTS-2077 oscilloscope using a successive approximation technique that samples the voltage at each point with 10ps time resolution. The DTS-2077 oscilloscope plot has a 10ps hardware resolution versus less than 1fs resolution on the Histogram (800fs/6000 samples) and 100fs on the CS803 (10ps / 100 hits). The user can choose to average the Oscilloscope Tool plots on the DTS by selecting the Passes to Average selection in the Options menu of the *Virtual Instruments* Oscilloscope tool version 3.00 and higher. For the purposes of making a quick measurement to see if the value is "in the ballpark," a 10ps scope tool resolution is more than adequate.

Bandwidth Calculations

Often, there is the need to correlate rise time measurements from two different instruments. A 20GHz plug-in has exceptionally good bandwidth for measuring a 300-400ps rise time. In a single pole driver model, with an assumed linear rise time, the bandwidth needed to accurately measure a 300ps rise time can be found from the equation:

BW = 0.35/RiseTime **eq. 1**
BW needed = 1.16 GHz

With a specified input bandwidth of greater than 2GHz, the DTS-2077 can accurately measure the rise times specified in the LVDS standard.

For a detailed discussion of bandwidth requirements, please refer to Appendix A.

Rise Time Measurement Conclusions

The equations in Appendix A demonstrate that the DTS-2077 and the CS803A will correlate within 2.5% on any 10%-90% rise time measured with the 1GHz P6247 differential scope probes. The two instruments measured almost exactly the same values. How was this achieved?

The actual device measurements were taken at the 20%-80% point of the signal as measured by the 20GHz instrument. Using the compare voltages from the highest bandwidth instrument allows the best observation of the signal. If we use Pulse Find to set the levels, an error resulting from the attenuation in the peak-to-peak values occurring in the lower bandwidth instrument is introduced. This error would understate the rise time values since the peak levels are lowered and the 20%-80% voltages closer together.

For the DTS-2077™, the most important signal specification for making rise time measurements is the comparator slew rate. The DTS-2077, with matched user threshold levels and at least 100mV of comparator overdrive, approaches the 20GHz bandwidth with respect to the slew rate of the input signal. If the slew rate of the signal does not have enough linear overdrive, the 2.5% error calculated in Equations 10 and 11 will be seen.

Fall Time Measurements

Differential fall time measurements were made in the same manner as the rise time measurements. Figure 12 shows the fall time using a DTS-2077 and the Oscilloscope tool in *Virtual Instruments*™. See Figure 8 for an illustration of this specification.

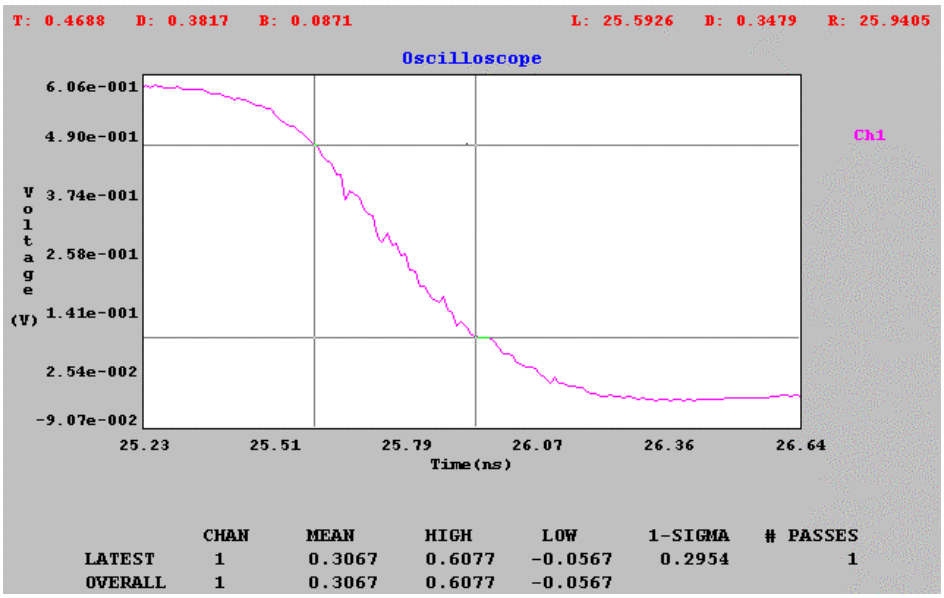


Figure 12 - Differential Fall Time into 100Ω Termination

Figure 13 is a plot using a CS803A communications analyzer with a 20GHz sampling head.

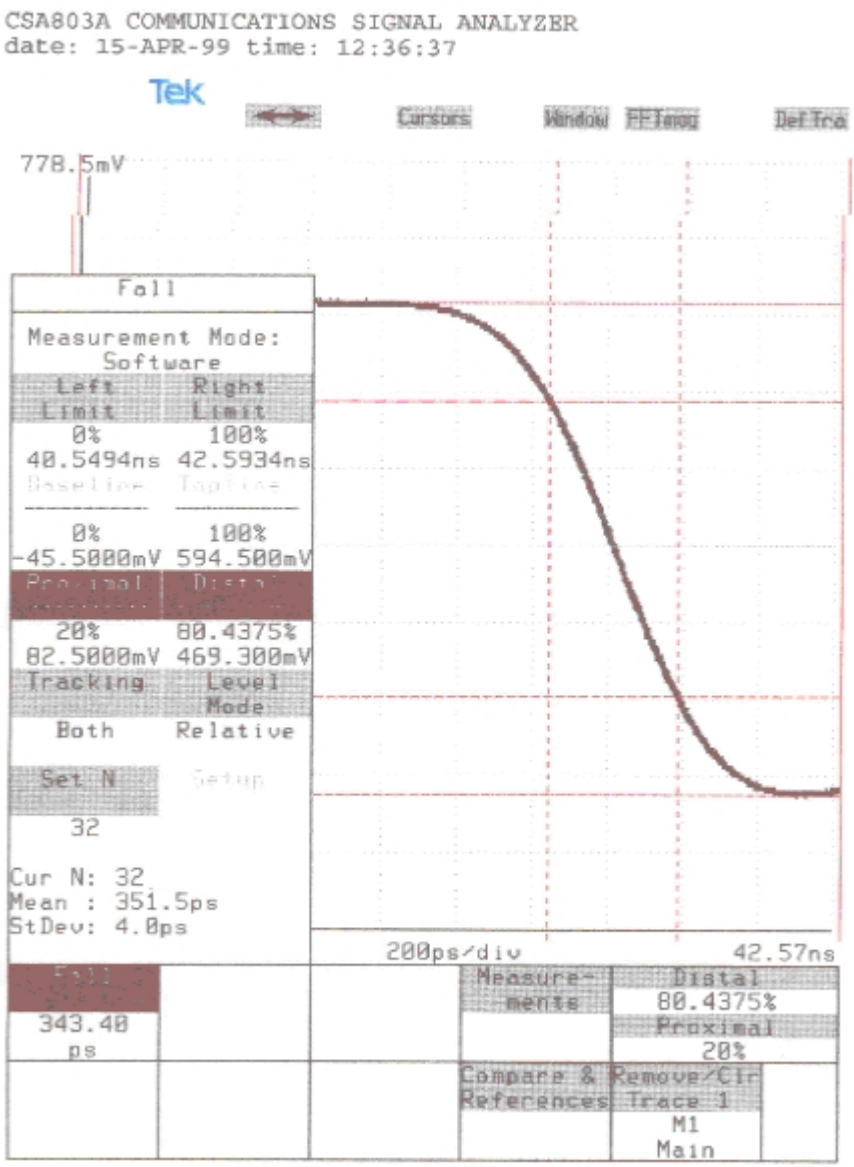


Figure 13 - CS803A Fall Time Measurement

Histogram Tool Measurements

Figure 14 is a simple histogram plot of the fall time (t_f) using the following setups in the Function Dialog pull-down menu of the Spectrum Tool:

Function..... TT- (*Transition Time Negative)*
Channel..... 1
Start Voltage..... 0.469
Stop Voltage..... 0.0825
Sample Size..... 6000
Pulse Find %..... USER
Arming..... Arm on Stop
Start Arming Event 1
Stop Arming Event 1

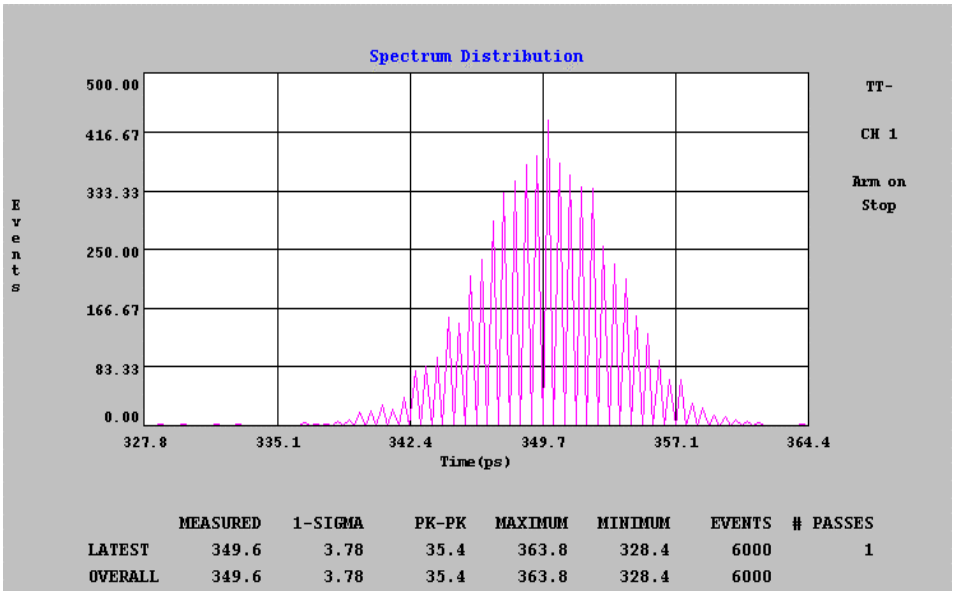


Figure 14 - Fall Time Histogram

The histogram reads 349.6ps for the measured value versus the scope measurement. The correlation values are displayed in Table 2.

CS803A	DTS-2077 Histogram	DTS 2077 Oscilloscope
343.00 ps	349.6 ps	348.0 ps

Table 2 - Correlation of Differential Fall Times

The correlation between the DTS-2077™ Oscilloscope measurement and the CS803A scope is much closer. This is due to the greater care taken in positioning the scope markers. All three measurements correlate well and are within the models set out in Equations 1-11.

Input to Output Propagation Delay

The input to output delay on an LVDS driver is defined as the time interval between the 50% voltage point on the input signal and the 50% point of the differential output rise time. Figure 15 is a timing diagram of how this T_{PLH} (Prop Delay Low to High Level Output) and T_{PHL} (Prop Delay High to Low Level Output) are measured.

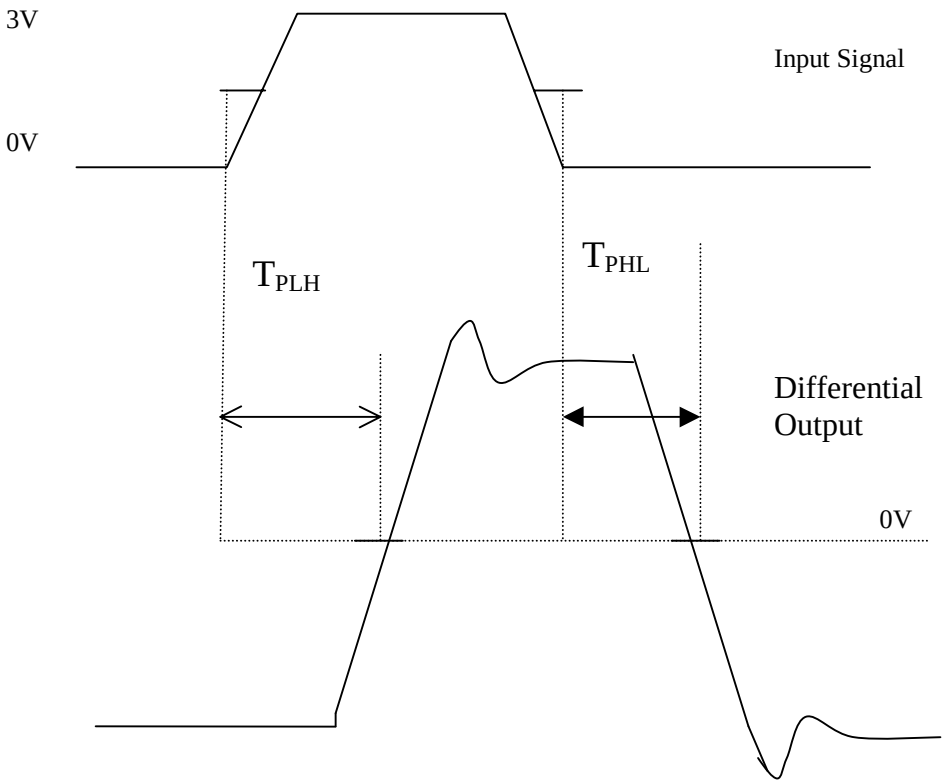


Figure 15 - Propagation Delay Measurement Signal Diagram

Figure 16 shows the test setup.

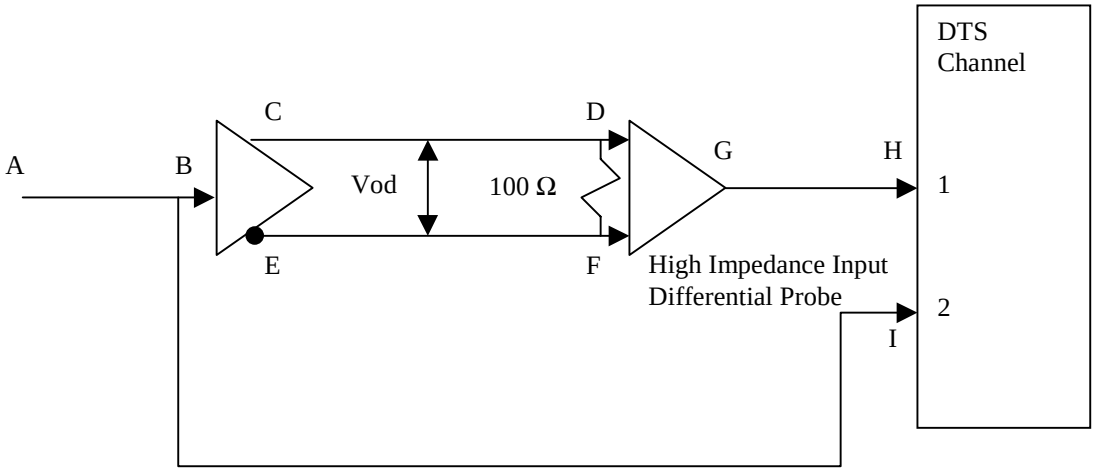


Figure 16 - Test Setup for Prop Delay Measurements

In order to accurately measure the signal at point B to the differential output between C and E, the input to output interface delays *must* be deskewed. This is done by nulling out the time delta between channels H and I while accounting for the delays C/D and E/F add to the measurement.

Ideally, the differential prop delay must be measured between point B and C-E at the Device-Under-Test (DUT). Automatic Test Equipment has, historically, used Time Domain Reflectometry (TDR) to offset the path lengths in the measurement. Often, on a lab bench, discrete measurements must be made of these signal delays while accounting for the errors in the measurements.

The DTS-2077™ can measure and store the path length differences. When an active probe like the P6247 is used, it is recommended that the External Cal with DC offsets selection from the Calibration Menu to account for the differences in the signal paths. When this was done, a skew of less than 20ps between signals was achieved.

Figure 17 is a TPD++ measurement for the two signal paths. Ideally this value should be 0. This picture was taken with the Tail-fit™ option of the Histogram Tool enabled in the VISI 5.0 software. A regular histogram would also suffice.

Function.....	TPD ++	(*Rising Edge on Channel 1 to Rising Edge On Channel 2)*
Channel.....	Both	(*Default*)
Start Voltage.....	0.2000	
Stop Voltage.....	0.2000	
Sample Size.....	6000	
Pulse Find %.....	50%-50%	
Arming.....	Arm on Start	
Start Arming Event ...	1	
Stop Arming Event ...	1	

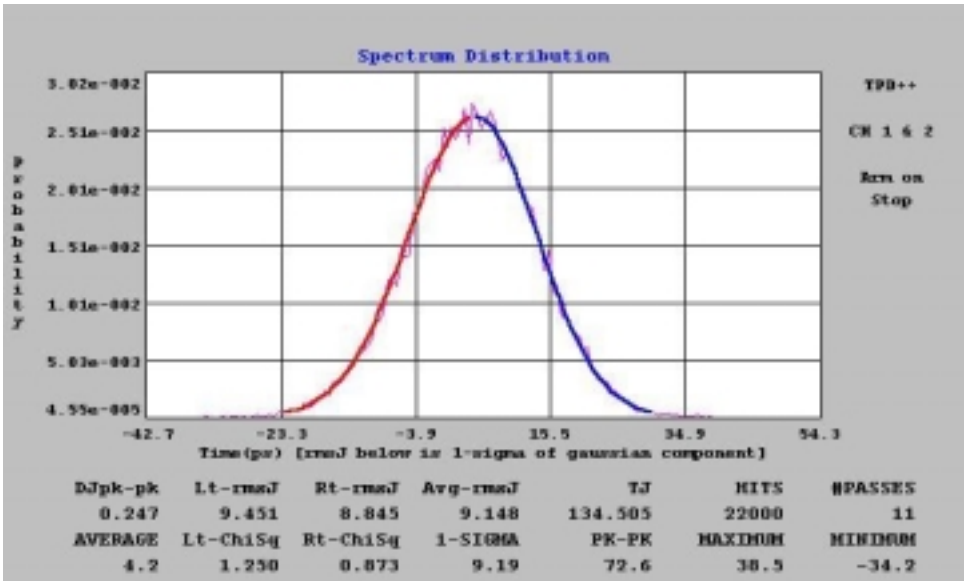


Figure 17 - Measurement of Skew Error after Calibration

The measured skew between the input signal that is measured through a coaxial cable and the Differential scope probe is only 4.2ps seen in the highlight box. The rest of this plot reveals the random jitter and common mode deterministic errors between the two signals. The gaussian or random error in the distribution is 9.15ps. A 50Ω coaxial cable is used to measure the input signal and a 1GHz differential probe is used to measure the outputs. The resulting skew is very good considering the potential for uncorrectable errors in active probes.

Once the probes are deskewed, the delta time between the probe point and the DUT pin(s) need to be reconciled. The time difference from the probe point to the DUT Pin is added to the resulting propagation delay value. Figure 18 shows an oscilloscope plot taken with the DTS-2077™ of T_{PLH} when the probes were placed directly on the device output and input pins.

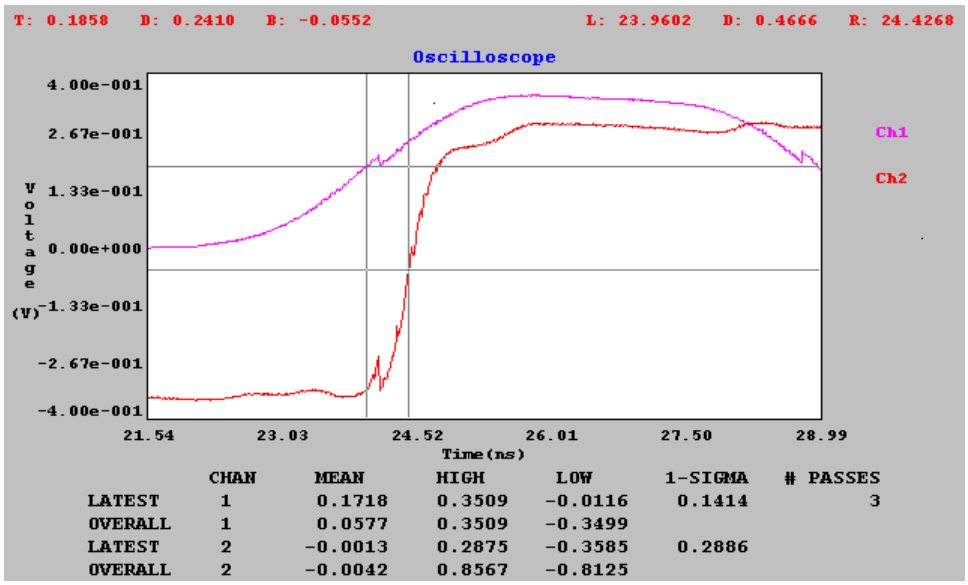


Figure 18 - Oscilloscope Picture of Waveforms and T_{plh}

Figure 18 shows the edge-to-edge performance of the LVDS driver device. The specification for this parameter is typically about 1.4ns with a minimum of 500ps.

Figure 19 is a Histogram plot of the TPD++. The measurement was taken using the 50% level. Since this is a two-channel measurement, a common mode error might occur due to bandwidth limitations and will be canceled out assuming that the performance of the input drive signal to the output drive signal is comparable. An input signal with excessive overshoot, or one that is much slower than the output signal, will introduce a voltage error in the selection of the 50% point when using the DTS-2077's **Pulse Find** function.

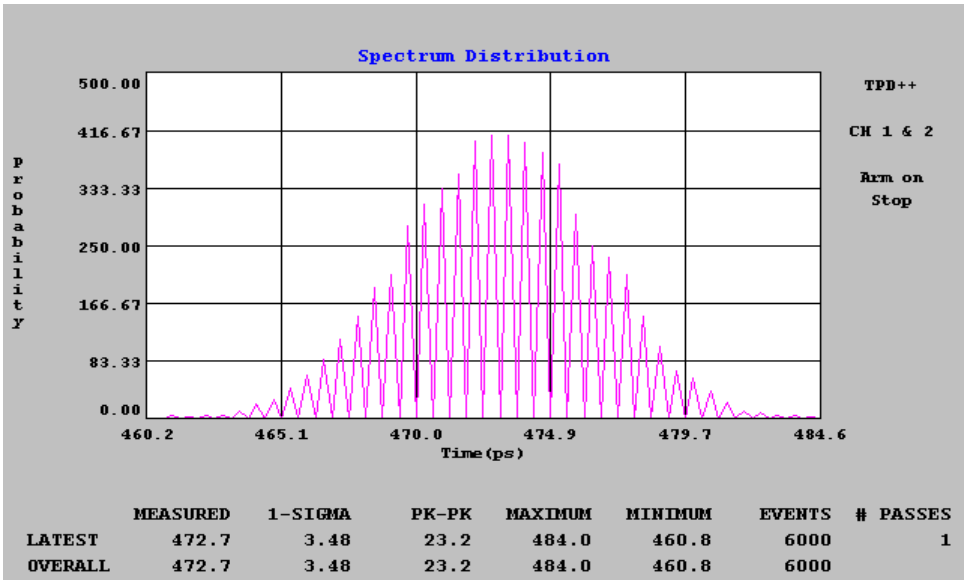


Figure 19 - Histogram of Input to Differential Output Signal on the DTS-2077™

Figure 20 is the correlation of this measurement to the 20GHz oscilloscope and demonstrates the excellent ability of the DTS-2077™ to make accurate channel-to-channel measurements.

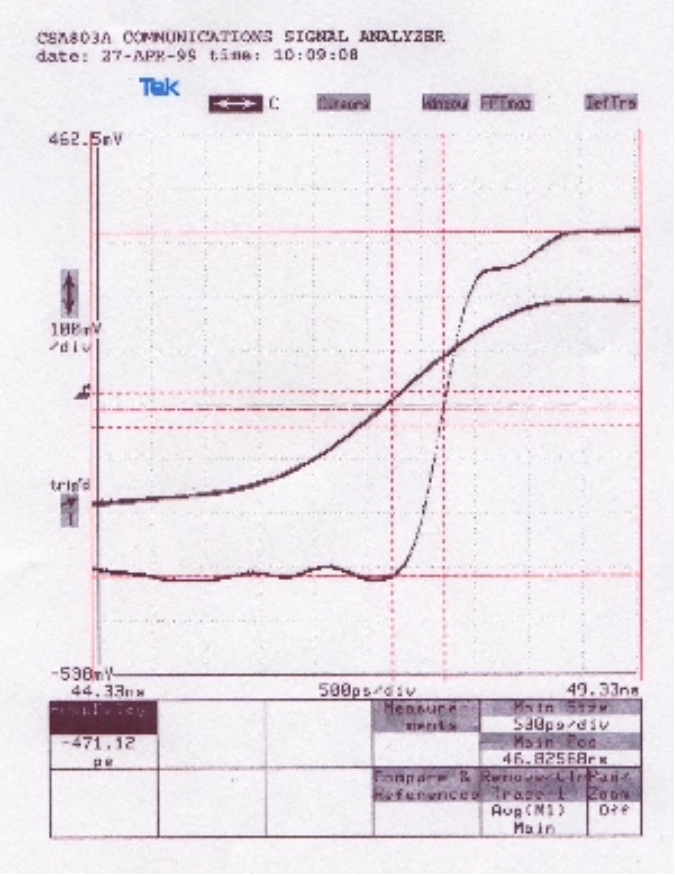


Figure 20 - Propagation Delay Measured on the CS8083A Oscilloscope

Table 3 is the correlation of T_{PLH} among the three methods used to make this measurement.

CS803A	DTS-2077 Scope	DTS 2077 Histogram
471.1ps	466.00ps	472.7ps

Table 3 - Prop Delay Correlation Low to High

The value on the CS803A scope is negative because the measurement is referenced from the output signal and the input signal is used as the reference on the DTS-2077 measurements. Also, the input signal has a 20dB (divide by 10) attenuator on the 3 Volt input signal to meet the DTS-2077 specification of +/- 1.1 volt input swings. The output of an LVDS driver is well within the comparator limits so no attenuation is needed on these output signals

Measuring T_{PHL}

The measurements for T_{PHL} are made in the same manner. The correlation results are shown in Table 4.

CS803A	DTS-2077 Scope	DTS 2077 Histogram
1.43ns	1.43ns	1.425ns

Table 4 - Prop Delay Correlation High to Low

These values meet the specification for this device with typical T_{PHL} values of 1.7 ns.

Channel to Channel Output Skew Characterization

Another important timing specification that the LVDS driver must meet is the Y (Out+) to Z (Out-) skew for the differential driver. These are specified to be no more than 300ps and typically values approach 0ps. The setup for this measurement is shown in Figure 21.

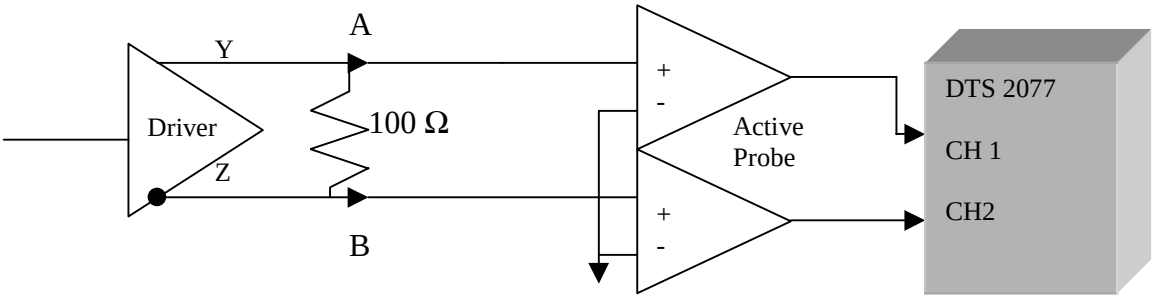


Figure 21 - Skew Connection Hook-up

With this setup, Tskew (o) is measured directly by taking the TPD+- and TPD-+ measurements between point Y and Z with deskewed probes. The function TPD+- measures the skew between the rising edge on channel 1 to the falling edge on channel 2. When TPD-+ is selected, the DTS-2077™ measures the time difference between the falling edge on channel 1 to the rising edge on channel 2. The comparator threshold is set to zero so the measurement is, in effect, measuring the zero crossing skew for the differential driver. Zero crossing skew results in Duty Cycle distortion at the receiver.

Figure 22 is the *Virtual Instruments*™ oscilloscope plot of the rising output on Y to the falling output on Z.

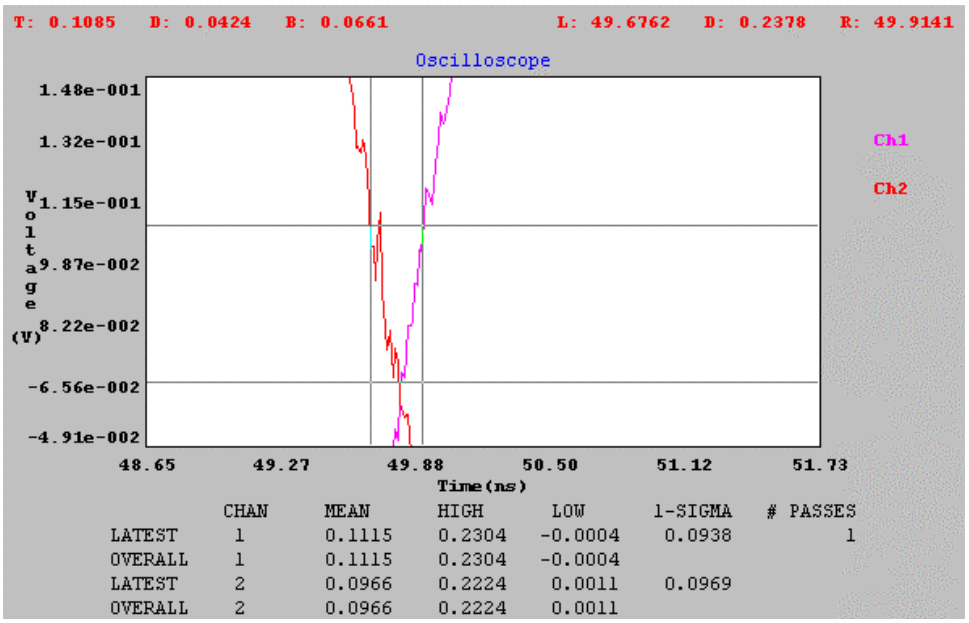


Figure 22 - Z to Y Output Skew

According to this scope picture, the falling edge on Z is 237ps earlier than the rising edge on Y. If we take a histogram to acquire a more accurate measurement we see that Figure 23 gives us a skew measurement of -230ps with a large pk-pk value of 86ps. This histogram has the following setup parameters:

Function..... TPD +- (*Rising Edge on Channel 1 to Falling Edge On Channel 2)*

Channel..... Both (*Default*)

Start Voltage..... 0.1111 0.1100 (*Grayed out since the 50%-50% Stop Voltage PulseFind Levels are used.*)

Sample Size..... 10000

Pulse Find %..... 50%-50%

Arming..... Arm on Start

Start Arming Event ..... 1 *(First Rising Edge)*

Stop Arming Event ..... 1 *(First Falling Edge)*

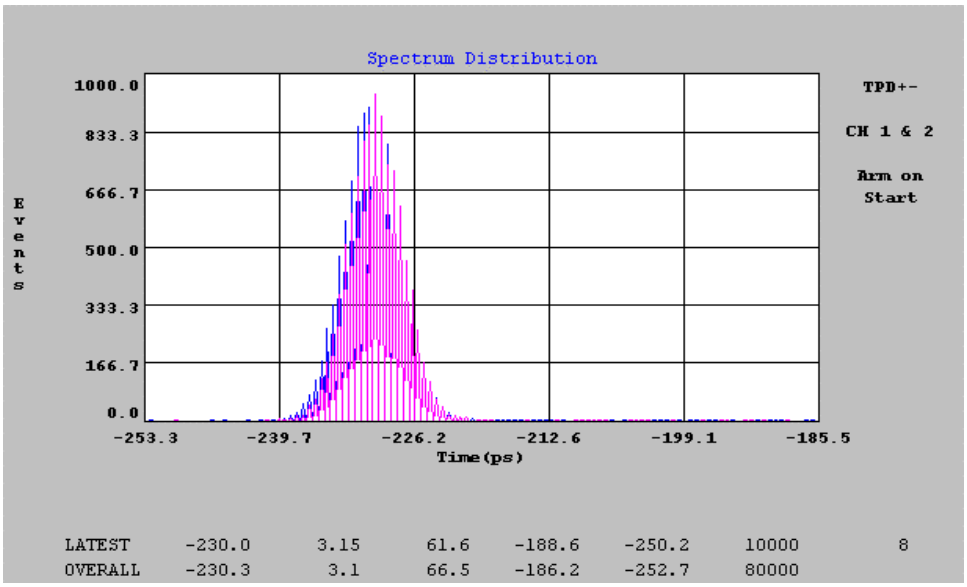


Figure 23 - Rising to Falling Y-Z Common Mode Skew

The falling to rising histogram in Figure 24 gives us a skew of +294ps. It is important that the skews for rising and falling edges be offset with opposite polarities. This reduces the common mode skew to 64ps and improves the average duty cycle performance of the LVDS driver.

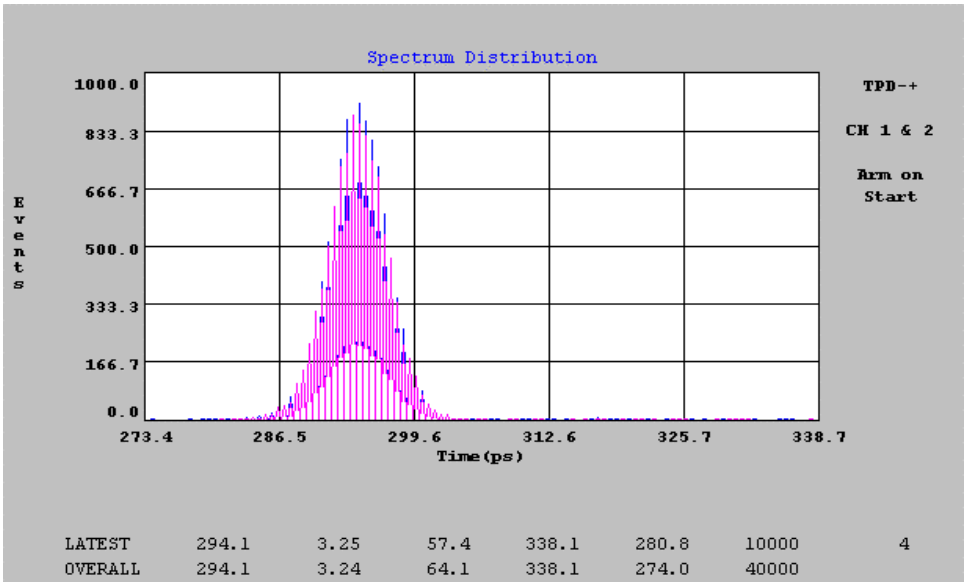


Figure 24 - Falling to Rising Edge Y-Z Common Mode Skew

Testing Jitter Generation and Jitter Transfer on an LVDS Driver

The LVDS specification does not deal with jitter generation or jitter tolerance specifications but the literature on LVDS devices does deal with this subject. In any system design, it is necessary to understand the stochastic process that affects point to point communications buffers. A properly designed timing budget that insures compliant operation and error free communication is only possible if the jitter of each component in the path is well understood. The DTS-2077™ with *Virtual Instrument*™ software, version 5.0 or greater, has a number of tools that make the separation of jitter components and the measurement of signal integrity possible. Using the patented tail fit algorithms in the Virtual Instrument software, the user can characterize the random and deterministic components on clock signals. The statistical processes of the random jitter, as well as the bandwidth limiting effects of the LVDS driver that is transmitting a pseudo-random bit stream, can be measured when using the data communications package in this software.

Jitter Measurement Setup and Procedure

The measurement setup for jitter generation on the LVDS transmitter is shown in Figure 25. The source used in this experiment was a pattern generator capable of generating up to 1.0625GB/s and injecting known amounts of jitter on the digital single-ended input to the LVDS driver. Two types of signals were used; a clock signal and a 2^7-1 PRBS (pseudo-random bit stream) pattern. The clock signal allows us to measure any periodic jitter and perform a Tail-fit™ on the histogram to measure the random jitter. The PRBS pattern allows us to measure the generation of DCD and ISI (Duty Cycle Distortion and Intersymbol Interference).

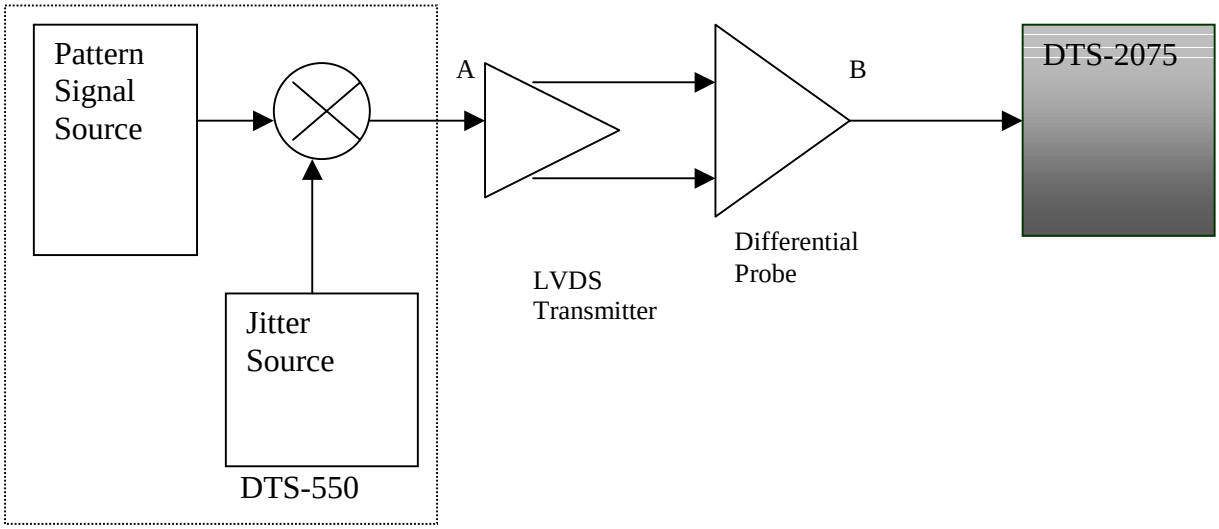


Figure 26 - Jitter Generation Measurement Setup

The jitter was first measured on the input to the LVDS Transmitter at Point A using a clock signal with the frequency varied from 100MB/s to 500MB/s in 50MB/s steps. This technique should expose any frequency dependent jitter. The next step was to make the same measurements on the output at B and plot the difference in the Deterministic

Jitter and Random Jitter that was measured in the Tail-fit™ of the clock period histogram. This should result in a jitter generation versus frequency plot.

Figure 27 is the jitter of the input clock signal running at 250MHz (500MB/s) measured with Tail-fit algorithms in the Spectrum Distribution window of *Virtual Instruments*™ Signal Integrity™ 5.0.

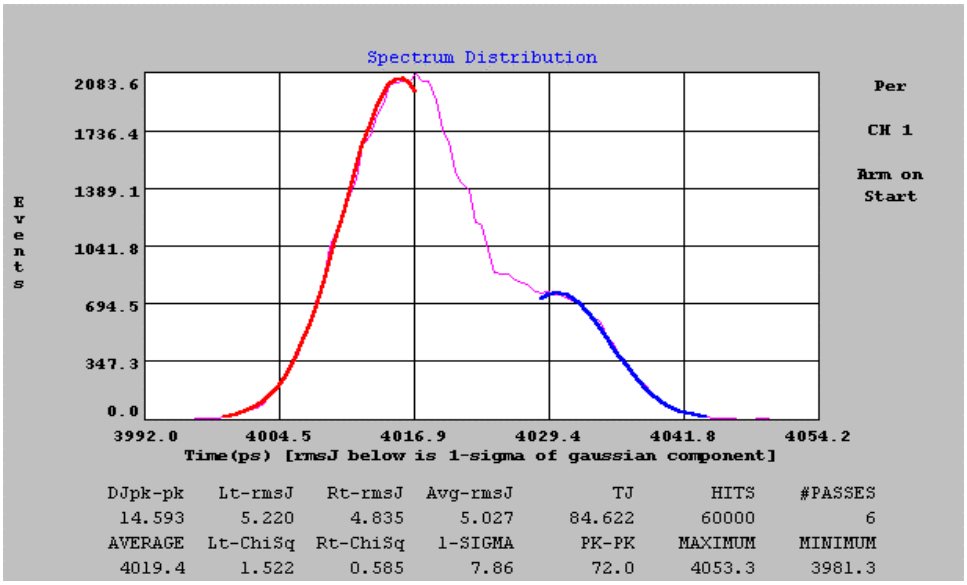


Figure 27 - Clock Input Jitter

It should be obvious from observing the plot in Figure 27 that the distribution of the clock periods is not a Gaussian function. When the histogram is not Gaussian, the one-sigma measurement is meaningless, except as a figure of merit. Calculating a 14-sigma value from the one-sigma measurement on this plot produces a value of 110ps (7.86ps *14). This is not the correct way to look at jitter since the one-sigma number is incorrect and the peak-to-peak number reveals nothing about the unbounded nature of the random jitter.

This plot displays two very important jitter measurements for calculating the correct total jitter. The first is the peak-to-peak deterministic jitter. *Virtual Instruments* reports 14.593ps of peak-to-peak Deterministic Jitter. Deterministic Jitter is the non-Gaussian portion of the jitter histogram and is bounded. The unbounded portion of the jitter is 5.027ps and represents the average of the left (red curve) and right (blue curve) sides of the Gaussian components of the histogram. The total jitter number is obtained by adding the deterministic to the random *N, where N is equal to a value calculated to produce the desired Bit Error Rate. In the case of a purely Gaussian distribution, a Bit Error Rate of 10^{-12} .is equal to 14 sigma.

Figure 28 shows the output of the LVDS transmitter.

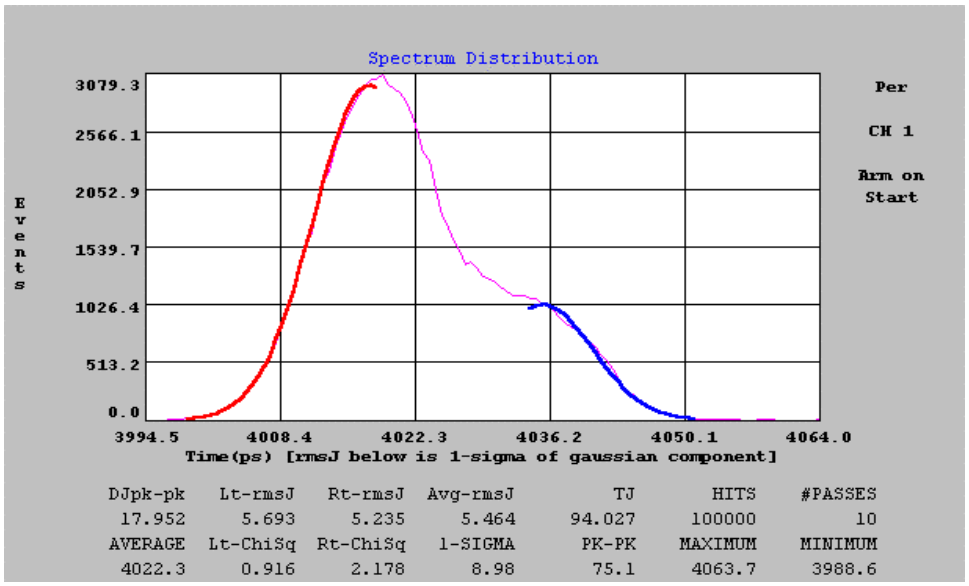


Figure 28 - LVDS Transmitter Output Jitter on Clock Signal

At this frequency, the clock signal passes through the LVDS buffer with very little added jitter. The Deterministic jitter goes up by 3.4 ps and the random jitter increases by 400 femtoseconds. The Total jitter increases by less than 10 ps. This jitter performance can now be compared to other buffer technologies and added to the system jitter budget.

The graph in Chart 1 is an Excel plot of the jitter generation of a clock signal for the LVDS transmitter over frequencies from 150 to 400 MHz.

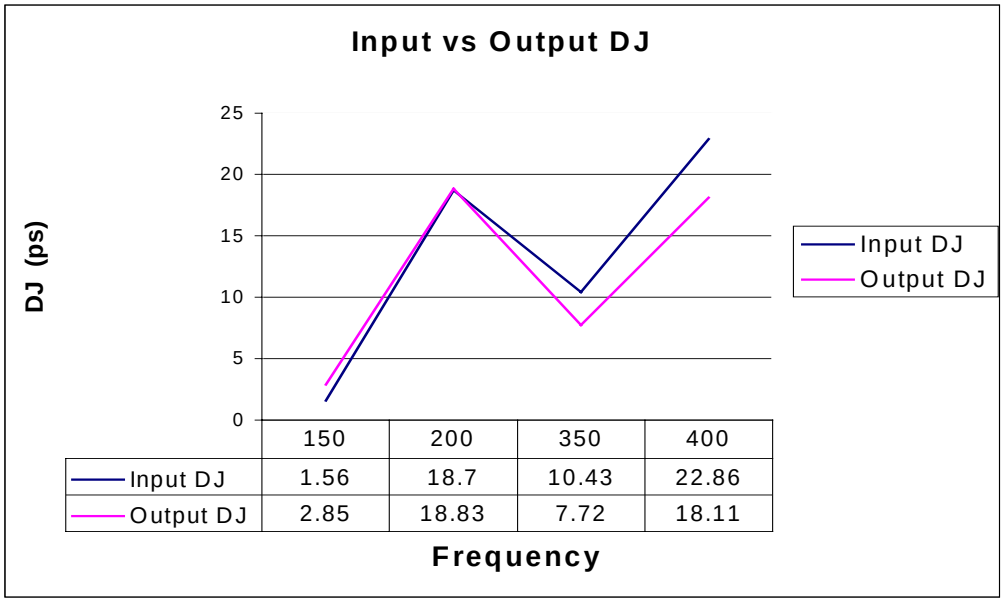


Chart 1

Note the reduction of DJ at higher frequencies caused by common mode Duty Cycle distortion.

The random Jitter is plotted in Chart 2.

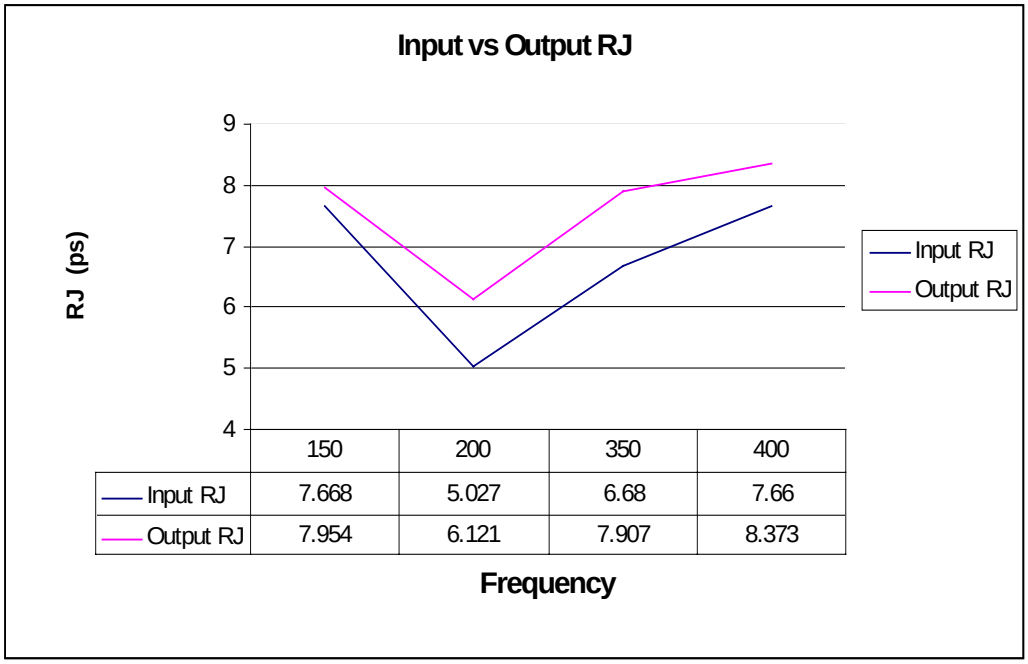


Chart 2

This plot shows that the LVDS driver adds about 1.5ps of random jitter. Over a 14-sigma test, the total random jitter added by the LVDS driver is about 21ps. Table 5 is the total jitter generation at each frequency with a BER of 10^{-12}.

150 MHz	200 MHz	350MHz	400 MHz
8.534ps	19.43ps	23.56ps	5.30ps

Table 5 - Total Transmit Jitter Generation for a Clock Signal

Jitter Generation for Data Patterns

If an LVDS part is used to transmit data, it is important to characterize the pattern dependent jitter produced by the transmitter. For this test, the pattern source is set to generate a 2^7-1 PRBS pattern. This pattern produces seven different frequencies of pulse widths in the data stream, the longest being seven Unit Intervals long. Any rise or fall time distortion from inter-symbol interference, effects that show up from pulse memory and the limited bandwidth of the transmitter will show up when the data output jitter is measured.

The pattern source is swept from 100MB/s to 500MB/s in 50MB/s steps and the total jitter is measured using the *Virtual Instruments*™ software dataCOM tool. Figure 29 is the input data jitter for the PRBS pattern measured at 400 MB/s. This jitter is made up of 59.475ps of Duty Cycle Distortion and Inter-Symbol Interference with 15.968ps of periodic jitter at the Nyquist rate of 200MHz.

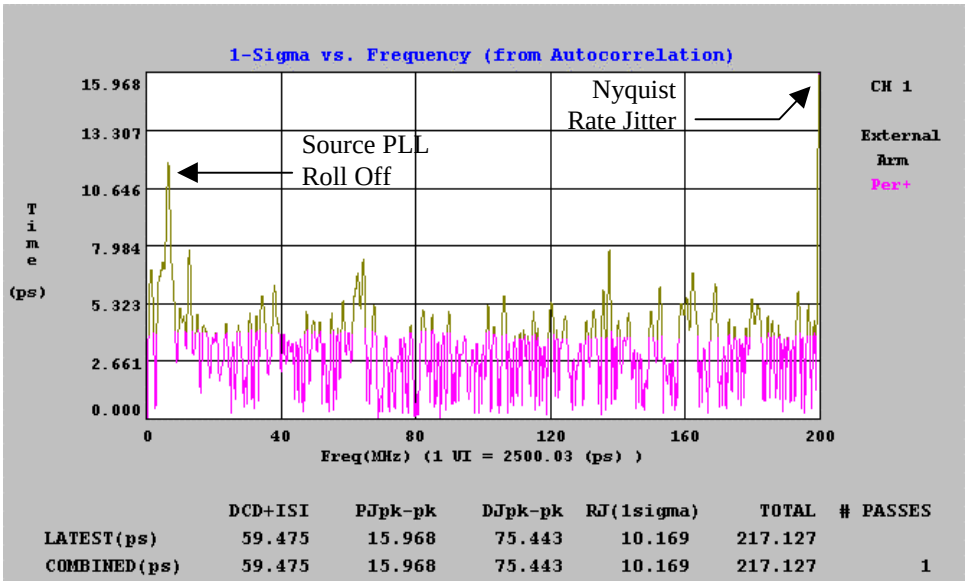


Figure 29 - Input Jitter on a 400MB/s Data Pattern

Figure 30 is the output of the LVDS transmitter at 400MB/s. Note how the DCD+ISI number went up by 115ps. This indicates that at 400MB/s, this part is introducing 115ps of edge placement distortion that was not seen in the case of a clock signal. This is the result of the difference in output propagation delays for rising and falling edges and any pulse memory effects generated by the part. Random Jitter increased only slightly by 700 femtoseconds. The periodic jitter increased by 2ps at the Nyquist frequency indicating some small effect of Duty Cycle distortion on the periodic jitter.

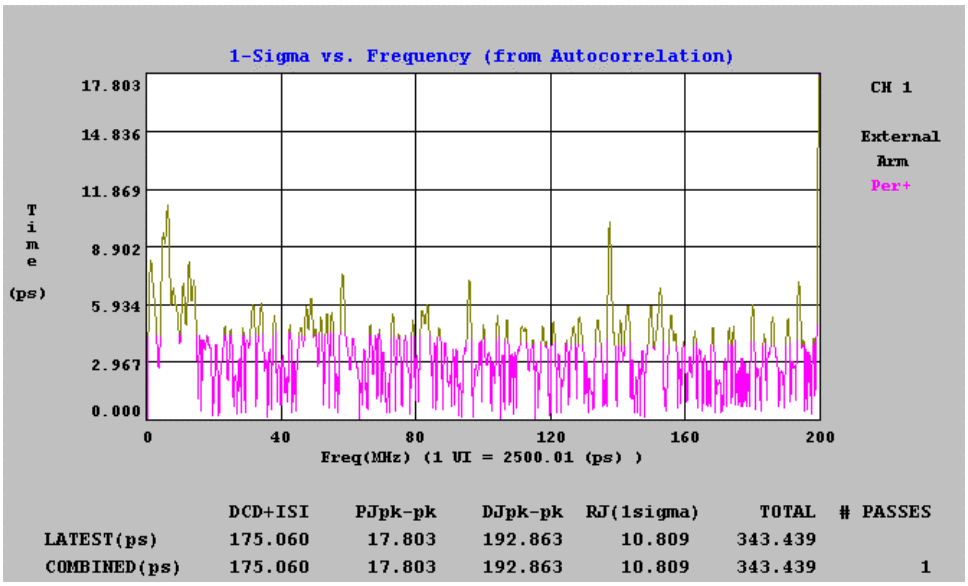
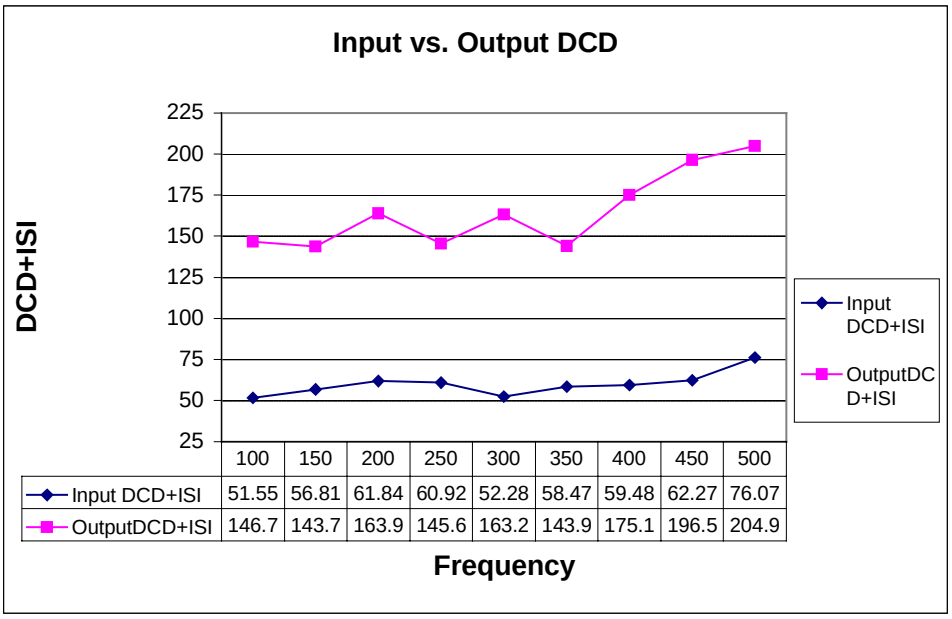


Figure 30 - LVDS Transmitter Output on a 400MB/s Data Pattern

Figure 30 shows the large increase in DCD and ISI including a small increase in periodic jitter on each of the FFT frequency spikes. The increase in total jitter measured at a BER of 10^{-12} is 116ps. Only 12ps of this difference is due to Random Jitter.

Chart 3 is a plot of the input to output transmitter DCD+ISI (Duty Cycle Distortion and Intersymbol Interference).

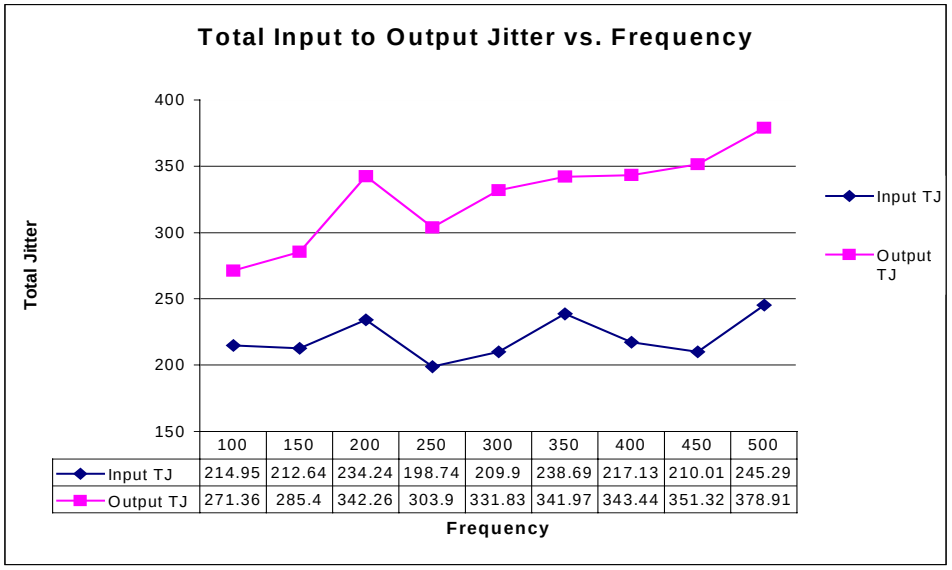


	100	150	200	250	300	350	400	450	500
Input DCD+ISI	51.55	56.81	61.84	60.92	52.28	58.47	59.48	62.27	76.07
OutputDCD+ISI	146.7	143.7	163.9	145.6	163.2	143.9	175.1	196.5	204.9

Chart 3 - DCD+ISI vs. Frequency

Note that as the part is pushed beyond its rated specification of 400MB/s, the DCD and ISI start to increase.

Chart 4 is a plot of the Input vs. Output Total Jitter.



	100	150	200	250	300	350	400	450	500
Input TJ	214.95	212.64	234.24	198.74	209.9	238.69	217.13	210.01	245.29
Output TJ	271.36	285.4	342.26	303.9	331.83	341.97	343.44	351.32	378.91

Chart 4 - Input vs. Output Total Jitter on Data Pattern

The total contribution of this LVDS transmitter to the total jitter budget is no more than 141ps across the operating range of this part. This is measured at 10^{-12} Bit Error Rate. Table 6 is the total jitter generation for the LVDS transmitter output.

100	150	200	250	300	350	400	450	500
56.413	72.765	108.018	105.155	121.928	103.279	126.312	141.308	133.619

Table 6 - Jitter Generation for PRBS Data Signal

Summary

This paper addresses the characterization of differential signals, specifically LVDS transmitter signals, into the 50Ω environment presented by *WAVECREST*'s DTS-2077™ and other high-speed instruments. The use of a 1GHz differential comparator in this case a Tektronix 6247 probe is essential for achieving the correct results. Successful measurements were obtained for AC parameters such as rise time, fall time, and propagation delay. Also addressed were characterization issues related to jitter generation and jitter transfer for both a clock signal and data patterns.

These are general techniques and should be applicable to the engineering methodology used for any device characterization. The results in this paper are best summarized in Tables 1-6. This paper also briefly touched on the Tail-fit™ capability of *WAVECREST*'s *Virtual Instruments Signal Integrity*™ 5.0 software.

Conclusion

Low Voltage Differential Swing transmitter technology does not require any peculiar or particularly difficult specifications for *WAVECREST*'s DTS-2077™ to measure and is an appropriate and accurate tool for measuring differential signals. VISI 5.0 software provides the right set of tools to characterize the transmitter timing specifications along with an extended ability to characterize the output jitter characteristics.

LVDS literature uses eye patterns and scope measurements to characterize jitter. The ANSI T11.2 jitter methodology requires parts to specify jitter at $10e^{-12}$ BER. This is a tough test problem requiring an in-depth understanding of all jitter components while utilizing an instrument that supports the proper methodology to characterize extremely low levels of jitter. The VISI 5.0 software and DTS instrument provide the engineer with a methodology, structure and capability to measure extremely low levels of jitter.

A High Bandwidth Digital Sampling oscilloscope can certainly measure the LVDS timing specification. The DTS-2077 or DTS-2075 brings the additional capability of making jitter measurements and accurately characterizing system timing margins quickly and accurately. In addition, these measurements can be made in a production test setup further enhancing the DTS-207x utility.

Appendix A - Instrument Bandwidth and Rise/Fall Time Measurements

Bandwidth Calculations

There is often the need to correlate rise time measurements on two different instruments. A 20GHz plug-in has exceptionally good bandwidth for measuring a 300-400ps rise time. The bandwidth needed to accurately measure a 300ps rise time is often approximated by the equation:

BW = 0.35/RiseTime or 1.16GHz **eq. 1**

The DTS-2077™, with a specified bandwidth of 2GHz, will have plenty of capability to measure the rise times specified by the LVDS specification.

Correlating Bandwidth Differences

When comparing the DTS-2077 to lower bandwidth instruments, a bandwidth adjustment calculation must be made. The typical bandwidth achievable on Automatic Test Equipment is in the 600MHz to 1GHz range. The most significant bandwidth limitation on ATE is the parasitic lumped capacitance on the signal path. Lumped capacitance results from ATE driver high impedance leakage, programmable load circuit capacitance and the pogo-to-via connections that create parasitics. Since it has already been shown that the 50Ω termination to ground does not work, a high-impedance load must be used. The high-impedance termination on an ATE comparator input typically contains at least 10pf of lumped capacitance. This capacitance slows the rise time of the signal.

The transient response of a signal in a 600MHz Bandwidth system is:

T_{rise} = 0.35/600MHz or 583ps **eq. 2**

The Transient Response of a 2GHz comparator is:

T_{rise} = 0.35/2GHz or 175ps **eq. 3**

These equations are only accurate for the single pole low-pass filter model of a comparator. Nevertheless, if the signal to the comparator has plenty of overdrive (>50mV) and the probe bandwidth is assumed to be infinite, we can use equation 3 to calculate T_{rise} of a 300ps rise time as seen by both a 2GHz and 600MHz comparator.

$$\text{Rise Time} = \sqrt{(\text{Instrument Rise Time})^2 + (\text{Signal Rise Time})^2} \quad \textbf{eq. 4}$$

Plugging in the values found in equations 2 and 3.

Rise Time Measured by 600MHz ATE comparator.

$$\text{Rise time} = \sqrt{(583\text{ps})^2 + (300\text{ps})^2} \qquad \textbf{eq. 5}$$

= 655 ps.

Rise Time Measured by 2GHz comparator

$$\text{Rise Time} = \sqrt{(175\text{ps})^2 + (300\text{ps})^2} \qquad \textbf{eq. 6}$$

= **347ps**

Rise Time Measured by a 20GHz sampling head

$$\text{Rise Time} = \sqrt{(50\text{ps})^2 + (300\text{ps})^2} \qquad \textbf{eq. 7}$$

= 304ps

Clearly, the input bandwidth of the measurement instrument has a huge impact on the ability of the system to properly measure rise time. How were the 20GHz scope and 2GHz comparator correlated on the DTS-2077?

Properly correlated results must include the bandwidth of the probe. The bandwidth of the P6247 differential probe is 1GHz. Using the hypothetical 300ps rise time, add in the 1GHz BW probe and the results.

600MHz ATE comparator with 1GHz differential Probe

Rise Time = .35/1GHZ =

$$\text{Rise Time} = \sqrt{(583\text{ps})^2+(350\text{ps})^2} \qquad \textbf{eq. 8}$$

679ps *instantaneous* rise time through a 600MHz comparator and P6247 differential probe.

Rise time of 300 ps signal:

$$\text{Rise Time} = \sqrt{(679\text{ps})^2+(300\text{ps})^2} \qquad \textbf{eq. 9}$$

The observable rise time for a 300 ps rise time input using these interface parameters is calculated to be:

742 ps measured rise time for ideal 300ps 10-90% transition.

Rise times much faster than 1ns at the 10-90% points cannot be measured through a 600MHz comparator and P6247, 1GHz differential probe.

2GHz DTS-2077 Comparator with 1 GHz differential Probe

$$\text{Rise Time} = \sqrt{(347\text{ps})^2+(350\text{ps})^2} \qquad \textbf{eq. 10}$$

492ps *instantaneous* rise time through a 2GHz comparator and P6247 differential probe

Rise time of 300 ps signal:

$$\text{Rise Time} = \sqrt{(492\text{ps})^2+(300\text{ps})^2} \qquad \textbf{eq. 11}$$

The observable rise time for a 300ps rise time input using these interface parameters is calculated to be:

576ps measured rise time for ideal 300 ps 10-90% transition.

20GHz CS803A DSO with 1GHz differential Probe

$$\text{Rise Time} = \sqrt{(304\text{ps})^2+(350\text{ps})^2} \qquad \textbf{eq. 11}$$

463ps *instantaneous* rise time through a 2GHz comparator and P6247 differential probe.

10-90% Rise time of an ideal 300 ps signal:

$$\text{Rise Time} = \sqrt{(463\text{ps})^2+(300\text{ps})^2} \qquad \textbf{eq. 12}$$

The observable rise time for a 300ps rise time input using these interface parameters is calculated to be:

551ps measured rise time for ideal 300ps 10-90% transition.

The reader is cautioned that these equations are a simplification of bandwidth requirements based on a single pole RC model for a driver. This equation ceases to be a good estimator when the rise time and fall times reach slew rates, where driver non-linearity becomes a factor. For example, source follower CMOS parts can have dramatically different rise and fall times and non-linear switching currents. Caution should be used for bandwidth estimates for parts with less than 200 ps rise times.

References

1. **National Semiconductor Application Note 1059 High Speed Transmission with LVDS Devices**

2. **National Semiconductor Application Note 1040 LVDS Performance: Bit Error Rate Testing Report #2**

3. **National Semiconductor Application Note 971 An Overview of LVDS Technology**

4. **National Semiconductor Application Note 977 Jitter Testing Using Eye Patterns Report #1**

5. **National Semiconductor Application Note 1088 LVDS Signal Quality: Cable Drive Measurements using Eye Patterns Report #3**

6. **Texas Instrument Specification SNLVDS31 High Speed Differential Line Drivers (slls261D) Copy right 1998**

7. **ANSI T11.2 Jitter Methodology**

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